

Dual-Stripline Configuration for Efficient Routing in Chiplet Interconnects

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Abstract

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Index Terms—bit error rate, crosstalk, dual-stripline, high-density interconnects, organic substrate

I. INTRODUCTION

THE increasing data transfer requirements of high-performance computing (HPC), artificial intelligence/machine learning, and other data center applications have necessitated the development of heterogeneous integration (HI) solutions. HI packages integrate chiplets/dielets manufactured in different fabs and technology nodes into a single system-in-package (SiP). This enables high-density, high-throughput data transfers with low latencies. To support such huge demands, HI utilizes interconnects with very fine pitch, including silicon interposers, silicon interconnect fabric, organic substrates, and embedded multi-die interconnect bridge (EMIB) platforms. These interconnects aim to achieve throughputs of around 1 Tbps/mm along the die edge, with energy efficiencies of 1 pJ/bit to 0.3 pJ/bit, and channel lengths of up to 50 mm, while maintaining latencies of less than 5 ns [1]. To facilitate high-density interconnects in die-to-die packages, two standards have emerged: the bunch-of-wires (BoW) interface from the ODSA-OCF community and the universal chiplet interconnect express (UCIe).

These standards enable interconnects routed in a single-stripline configuration, wherein different signal layers are

shielded by ground layers. The primary objective of these interconnects is to increase bandwidth density. Achieving a higher bandwidth density requires increasing the number of routing layers as the lines cannot run too close to each other due to mutual coupling between them. Each of these routing layers has to be separated by ground planes, which limits the overall routing densities and introduces manufacturing challenges as it results in a larger stack-up. The routing densities can be increased further by routing the signals in the dual-stripline configuration within the same stack-up, as opposed to the conventional single-stripline configuration. However, this can also lead to severe near-end crosstalk (NEXT) and far-end crosstalk (FEXT) issues due to the absence of ground shielding between adjacent signal layers. These crosstalk issues in dual-stripline routing have been studied before and some mitigation techniques have also been proposed in [2]–[5]. One method discussed in [2] is to reduce the NEXT and FEXT effects by employing new routing strategies that vary the inter-pair spacing. However, this method, while effective for differential pair to differential pair and differential pair to single-ended, results in lower routing density compared to the single-ended scheme. In the case of a single-ended configuration, the impact of crosstalk becomes more prominent. The paper [3] specifically focuses on the analysis of single-ended dual-stripline far-end crosstalk issues and proposes an optimized inter-layer crosstalk equation that characterizes the effect of vertical and horizontal offsets. However, these studies primarily concentrate on analyzing the dual-stripline structure in PCB board-level designs, particularly targeting low-density interconnects. Other studies, such as those mentioned in [4] and [5], explore novel routing strategies involving twisted pairs or angular bends to mitigate crosstalk problems. Nonetheless, these techniques require more space and result in lower-density interconnects. However, the feasibility of using the dual-stripline configuration for high-density interconnects has not been explored before.

In this work, we propose a dual-stripline configuration for high-density interconnect routing on an organic substrate. An 8-2-8 layer stackup is utilized with a half-pitch offset between adjacent layer signal traces. The dual-stripline configuration increases the number of signal routing layers within the same stackup, leading to a significant improvement in routing efficiency. It is important to note that this enhancement comes at the cost of increased crosstalk due to the absence of a ground layer between signal layers. To address these crosstalk issues and further enhance routing efficiency, we demonstrate through

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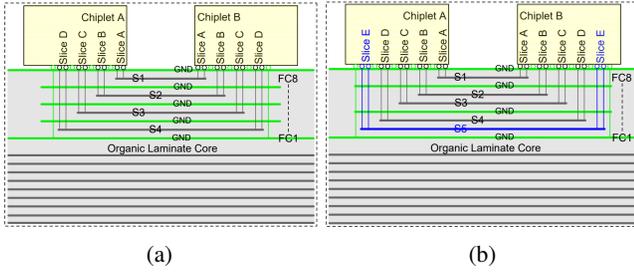


Fig. 1. Signal routing in the standard 8-2-8 stackup. (a) The conventional single-stripline configuration supports four signaling layers (S1-S4). (b) The proposed dual-stripline routing for die-to-die interfaces on the organic substrate supports an additional routing layer (S5 - Slice E), which increases the signal layer count within the same stackup.

simulations that by utilizing sufficient wire-to-wire pitch, the traces can be routed in the dual-stripline configuration with an offset between the two layers.

The remainder of this paper is organized as follows: Section II provides a comprehensive review of the dual-stripline configuration and its underlying principles. In Section III, we present the experimental methodologies and simulation setups used in our analysis for channel modeling and extraction. Section IV presents the time domain analysis for the dual-stripline configuration on the organic substrate. Finally, in Section V, we summarize our findings and provide recommendations for future research.

II. DUAL-STRIPLINE CONFIGURATION

Fig. 1(b) illustrates the reorganization of the stack-up by incorporating two signal layers between two ground layers. In a standard 8-2-8 stack-up configuration, the top 8 layers above the core are allocated for signal routing, while the bottom 8 layers serve as power and ground planes. In the conventional single-stripline structure within the top 8 layers (Fig. 1(a)) four layers are allocated for signal routing, each shielded by a top and bottom ground layer to mitigate inter-layer crosstalk. However, increasing the routing density in the single-stripline configuration would require adding more signal layers, resulting in a larger stack-up. This would escalate costs and introduce manufacturing complexities. To enhance routing density without these drawbacks, one of the ground layers can be replaced with a signal layer, resulting in a dual-stripline configuration (Fig. 1(b)). This additional signal layer increases the number of signal layers by one, thereby improving bandwidth density. In a general stack-up employing the dual-stripline structure, the overall routing density can be increased by 33%. Nevertheless, the dual-stripline configuration introduces more inter-layer crosstalk issues since each signal layer has only one ground shielding. The dual-stripline configuration can be implemented in two ways: one with signal routing lanes placed directly below each other, and another with lanes laid out with an offset of half the wire-to-wire pitch in one layer (Fig. 2(b), 2(c)). The offset

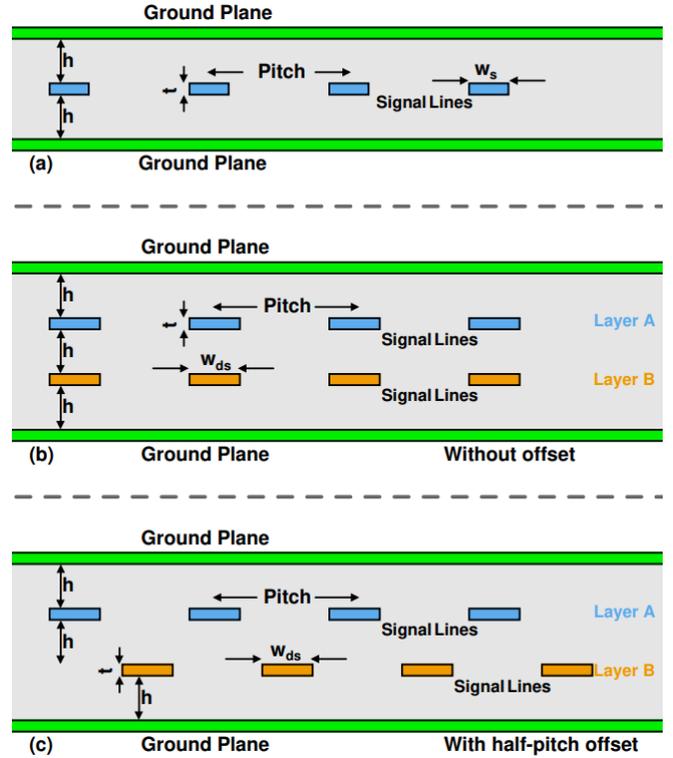


Fig. 2. Front (cross-sectional) views of (a) the conventional single-stripline configuration; (b) the dual-stripline configuration without offset; and (c) the dual-stripline configuration with a vertical offset of half the wire-to-wire pitch (i.e. 32.5 μm).

plays a crucial role in reducing the impact of crosstalk, as it influences the horizontal and vertical distances between the layers. Previous studies [2], [3] have analyzed the effect of offset variation on crosstalk values and determined the optimal point based on achieving the minimum crosstalk value. It has been observed that the minimum crosstalk point occurs when the traces are laid at a half wire-to-wire pitch offset.

Fig. 1 illustrates that each chiplet comprises multiple slices, which can be configured as either transmitters or receivers. Consequently, it is essential to consider two types of crosstalk effects: near-end and far-end crosstalk. In the co-propagating case, where all slices (slice A and B) in chiplet A are configured as transmitters, and in chiplet B as receivers, only the effect of far-end crosstalk needs to be taken into account (Fig. 3(a)). Conversely, in the counter-propagating case, both chiplets A and B have transmitters and receivers. For instance, slice A in chiplet A is configured as a transmitter, while slice B is configured as a receiver. Similarly, in chiplet B, slice A acts as a receiver, and slice B acts as a transmitter (Fig. 4). In this scenario, both far-end and near-end crosstalk must be considered (Fig. 3(b)). The near-end crosstalk is caused by transmitters in the adjacent signal layer, as there is no ground shielding between the signal layers. The resulting effective crosstalk effects from far-end aggressors on the same layer

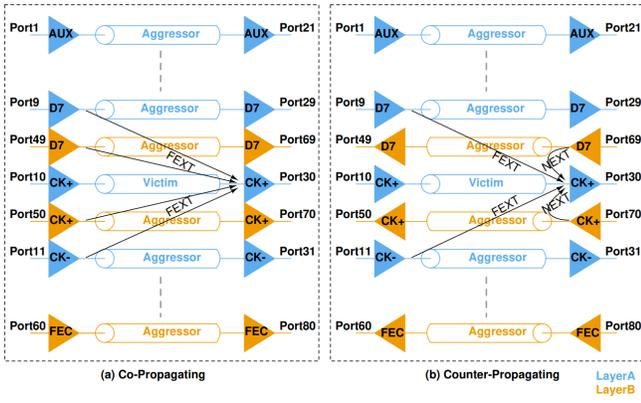


Fig. 3. The aggressor-victim topology for the dual-stripline simulations. (a) Co-propagating case wherein the transmitters in Layer A and Layer B are transmitting in the same direction. (b) Counter-propagating case wherein the transmitters in Layer A and Layer B are transmitting in opposite directions.

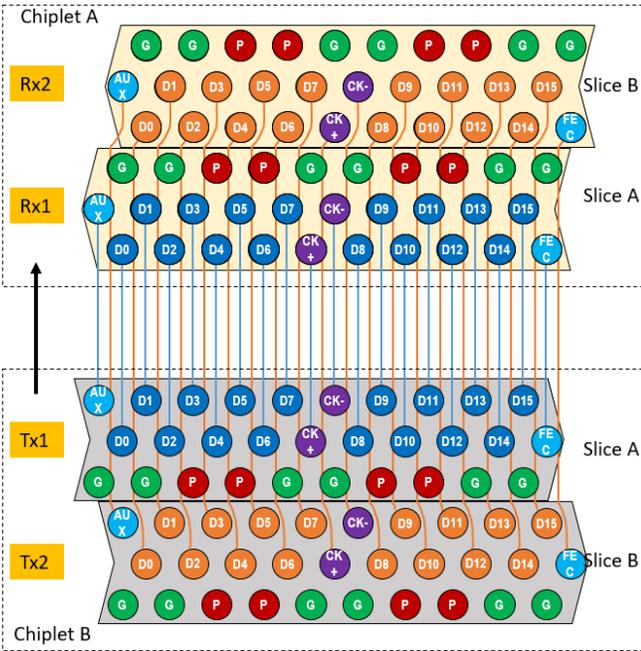


Fig. 4. Proposed bump-map for the dual-stripline co-propagating case with half-pitch offset (i.e. $32.5 \mu\text{m}$) for traces between Layer A (Slice A) and Layer B (Slice B).

and near-end aggressors from the adjacent layers are evaluated in terms of power sum crosstalk. In the following section, we present a simulation-based comprehensive analysis of the dual-stripline configuration and its impact on crosstalk reduction for high-density interconnects in organic substrates.

III. CHANNEL MODEL EXTRACTION

To investigate the efficacy of the proposed dual-stripline configuration for high-density interconnects, simulations were conducted on an organic substrate channel for the bunch-of-wires interface. In the case of an organic substrate with an

8-2-8 stack-up, the current BoW architecture supports four slices, where each slice has 16 data pins (D0 - D15), one forward error correction pin (FEC), one auxiliary pin (AUX) and two pins for differential clock (CK+ and CK-) as shown in Fig. 4. Typically, the signals are routed using a single-stripline configuration. Therefore, with the 8-2-8 stack-up and the single-stripline configuration, there are four signal layers, each responsible for routing one slice. Thus each slice can support a data rate of up to 256 Gbps [7] with a data rate of 16 Gbps per wire, resulting in a total bandwidth density of 1024 Gbps. By implementing the dual-stripline configuration in the 8-2-8 stack-up on an organic substrate, the number of signal layers increases to five, leading to a higher bandwidth density of 1280 Gbps. The BoW architecture on the organic substrate has a bump-to-bump pitch of $130 \mu\text{m}$ and with two rows of signal bumps (Fig. 4), the signal wire-to-wire pitch is $65 \mu\text{m}$. With this wire-to-wire pitch, the dual-stripline configuration can be employed in the BoW architecture, utilizing a half-pitch offset of $32.5 \mu\text{m}$ to mitigate inter-layer crosstalk effects. The vertical separation between the signal layers is $30 \mu\text{m}$. The chosen dielectric material is ABF (dielectric constant of 3.4, loss tangent of 0.019), and the copper rms roughness is $0.4625 \mu\text{m}$.

The channel physical parameters such as trace width and metal thickness for the BoW channel on an organic substrate for dual-stripline configuration were selected to yield a characteristic impedance of 50Ω for a channel length of 20 mm. Initially, the insertion loss and crosstalk effects of the dual-stripline structure, excluding the bumps and vias i.e. just the transmission lines (T-lines-only) between the two chiplets were characterized using Ansys HFSS (with 3D full wave simulation). Then to incorporate the impact of vias and bumps on the dual-stripline channel, S-parameters were separately extracted for the bumps and the vias. The dimensions chosen for the bump are $54 \mu\text{m}$ diameter, and $54 \mu\text{m}$ height. These extracted S-parameters are cascaded with the T-lines-only model to get the effect of the entire bump-to-bump model (Full model) for the dual-stripline structure.

Fig. 5 and Table I, presents a comparison of insertion loss, return loss, powersum FEXT, and powersum FEXT+NEXT values among the single-stripline full model structure, dual-stripline T-lines-only model, and the dual-stripline full model for the BoW structure in an organic substrate. The powersum crosstalk values are calculated using the equations (1) and (2) based on the individual crosstalk values, where 'n' refers to the port number of aggressors.

$$\begin{aligned} & \text{Powersum FEXT} \\ &= 10 \log \left(\sum_{n=1, n \neq 10}^{20} |S_{30,n}|^2 + \sum_{n=41}^{60} |S_{30,n}|^2 \right) \end{aligned} \quad (1)$$

$$\begin{aligned} & \text{Powersum NEXT+FEXT} \\ &= 10 \log \left(\sum_{n=1, n \neq 10}^{20} |S_{30,n}|^2 + \sum_{n=61}^{80} |S_{30,n}|^2 \right) \end{aligned} \quad (2)$$

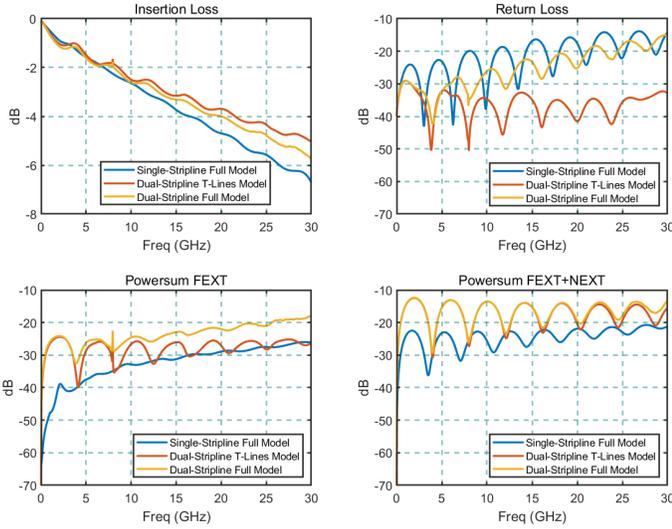


Fig. 5. Comparison of insertion loss, return loss, powersum FEXT and powersum FEXT + NEXT among the single-stripline (Full model), the dual-stripline transmission line model (T-lines-only model) and dual-stripline bump-to-bump model (Full model) of 20 mm channel on organic substrate.

TABLE I
COMPARISON OF S-PARAMETER VALUES

Channel	Insertion Loss(dB) @ 8GHz	Return Loss(dB) upto 16 GHz	Co-propagating case: Powersum FEXT(dB) upto 30 GHz	Counter-propagating case: Powersum FEXT+NEXT (dB) upto 30 GHz
Dual-stripline T-lines-only model	1.8	< -29.0	< -24.1	< -12.6
Dual-stripline full model	1.9	< -22.5	< -18.0	< -12.6
Single-stripline full-model	2.3	< -16.4	< -26.1	< -21.4

Note: With the addition of bumps and vias to the T-lines-only model to the dual-stripline the powersum FEXT degrades by 6dB

While calculating the powersum FEXT (1), we consider the slices to be configured in a co-propagating manner. On the other hand, for the powersum NEXT+FEXT (2), the slices are configured in the counter-propagating case. In both cases, we consider 19 aggressors from the same layer and 20 aggressors from the adjacent layer. The maximum value of powersum FEXT at 8 GHz, for the dual-stripline T-lines-only model, degraded by 1.9 dB due to coupling with the adjacent signal layer in comparison to the single-stripline full model structure. Moreover, the addition of bumps and vias degraded the crosstalk by another 4.5 dB.

As observed from Table I, the insertion loss of the dual-stripline T-lines-only model was reduced by 0.45 dB compared to the single-stripline full model in the BoW channel, remain-

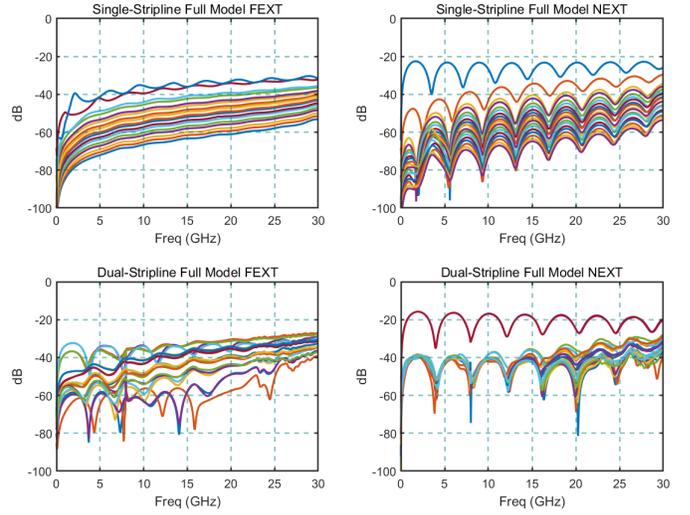


Fig. 6. Individual FEXT and NEXT values from all aggressors (same layer-19 and adjacent layer-20) of the single-stripline channel and dual-stripline 20 mm channel.

ing within the BoW specification value of 4 dB. The inclusion of bumps and vias with the T-lines-only model further deteriorated the insertion loss by 0.1 dB. Also, the maximum powersum FEXT value up to 30 GHz is -18 dB, which satisfies the BoW specification of below -15 dB. Additionally, in the counter-propagating case, the effect of NEXT becomes more pronounced due to the transmitters in the adjacent signal layer. Consequently, the summation of powersum NEXT and FEXT values exceeds the limits set by the BoW specification, as depicted in Fig. 5.

In Ref [9], for a single-stripline configuration in a homogeneous medium, the far-end crosstalk and the near-end crosstalk can be estimated by (3) and (4). Here K_{FEXT} is the far-end crosstalk coefficient, K_{NEXT} is the near-end crosstalk coefficient, V_f is the voltage at the far end of the quiet line, V_a is the voltage on the signal line, V_b is the voltage noise on the quiet line in the backward direction, Len is the length of the coupled region between the two lines, k_f the far-end coupling coefficient that depends only on intrinsic terms, k_b is the backward coefficient, RT is the rise time, v is the speed of the signal on the line, C_{mL} is the mutual capacitance per length, in pF/inch (C_{12}), C_L is the capacitance per length of the signal trace, in pF/inch (C_{11}), L_{mL} is the mutual inductance per length, in nH/inch (L_{12}), and L_L is the inductance per length of the signal trace, in nH/inch (L_{11}).

$$K_{FEXT} = \frac{V_f}{V_a} = \frac{Len}{RT} k_f = \frac{Len}{RT} \frac{1}{2v} \left(\frac{C_{mL}}{C_L} - \frac{L_{mL}}{L_L} \right) \quad (3)$$

$$K_{NEXT} = \frac{V_b}{V_a} = k_b = \frac{1}{4} \left(\frac{C_{mL}}{C_L} + \frac{L_{mL}}{L_L} \right) \quad (4)$$

When striplines are routed on a homogeneous medium, the capacitance-to-inductance ratio ideally approaches unity, leading to minimal far-end crosstalk. This effect was similarly

observed in the dual-stripline configuration, as described by [3], where the homogeneous medium also contributed to the ideal reduction of far-end crosstalk. However, upon examining simulation results (Fig. 6), it became apparent that finite levels of far-end crosstalk persisted in both the single-stripline and dual-stripline setups, measuring below -30.3 dB and -24.1 dB, respectively, up to 30 GHz. This finite far-end crosstalk was introduced due to disparities in even and odd mode resistances (R_{even} and R_{odd}) of the traces, calculated from resistance matrix using equations (5) and (6).

$$R_{even} = R_{self} + R_{mutual} \quad (5)$$

$$R_{odd} = R_{self} - R_{mutual} \quad (6)$$

$$\Delta R = R_{odd} - R_{even} \quad (7)$$

The resistance matrix values were obtained for a two-trace structure using ANSYS Q3D extractor for both single-stripline and dual-stripline models (detailed in Table II). Calculated values for R_{even} , R_{odd} , and ΔR using equations (5), (6), and (7) are presented in Fig. 7. In this figure, it is evident that non-zero ΔR values exist for both single-stripline and dual-stripline setups, resulting in distinct attenuation for even and odd mode signals. Since R_{even} consistently exceeded R_{odd} for all cases, even mode signals suffered greater attenuation than their odd mode counterparts [8]. Additionally, as the $|\Delta R|$ value increased, coupling also intensified, resulting in a finite amount of crosstalk. Furthermore, transitioning from a single-stripline to a dual-stripline configuration yielded higher ΔR values, signifying increased crosstalk in the dual-stripline setup. In the case of the dual-stripline configuration, inter-layer coupling prevailed over same-layer coupling. This enhanced inter-layer coupling was evident in time-domain simulations, particularly when assessing the FEXT component in both single-stripline and dual-stripline models. For these simulations, an input signal with an amplitude of 0.75 V, a pulse width of 42.5 ps, and rise and fall times of 20 ps are applied to one of the traces, and FEXT components on adjacent traces are monitored. As illustrated in Fig. 8, FEXT on the adjacent trace in a single-stripline setup was notably lower than in the dual-stripline configuration. Additionally, the inter-layer adjacent trace exhibited 7.5 mV of FEXT, while the same-layer adjacent trace recorded 4.8 mV in the dual-stripline configuration, indicating a more substantial coupling effect attributed to the higher ΔR value. Furthermore, it was observed that there existed a difference in the rise and fall times of the even and odd mode signals, measuring 0.04 ps and 0.07 ps for the same layer and inter-layer traces, respectively. Therefore, despite the medium being homogeneous, due to the difference in mode resistances and rise time values, a finite amount of crosstalk was observed in both the dual-stripline and single-stripline configurations. So, to mitigate crosstalk, it is crucial to increase both the inter-layer spacing and the trace spacing within the same layer. By doing so, the coupling strength can be reduced, resulting in a reduction in the disparity of rise and fall times. These adjustments effectively contribute to minimizing the extent of crosstalk interference.

TABLE II
RESISTANCE MATRIX FROM ANSYS Q3D EXTRACTOR

Resistance	Dual stripline		Stripline
	Same layer	Adjacent layer	
R11 (R_{self})	16.1 Ω	16.1 Ω	13.9 Ω
R12 (R_{mutual})	5.2 Ω	5.6 Ω	2.9 Ω
R21 (R_{mutual})	5.2 Ω	5.6 Ω	2.9 Ω
R22 (R_{self})	16.2 Ω	16.4 Ω	13.9 Ω

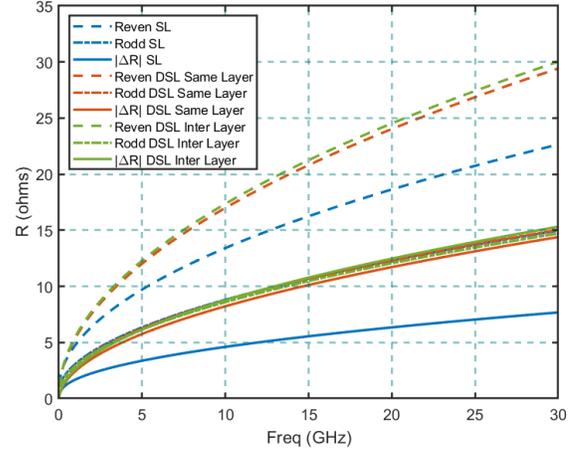


Fig. 7. Frequency-dependent even and odd mode resistances for stripline (SL) and dual-stripline (DSL) obtained using ANSYS Q3D Extractor.

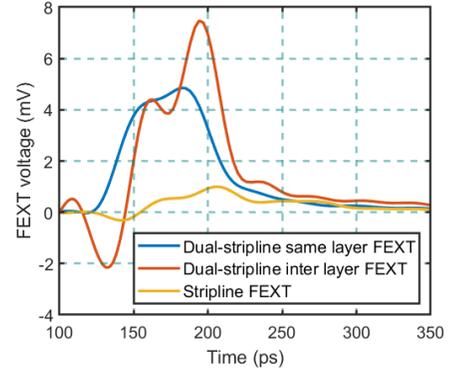


Fig. 8. Comparison of FEXT values: single-stripline and dual-stripline same layer and adjacent layer traces of a 20 mm channel on an organic substrate.

IV. TIME DOMAIN ANALYSIS OF DUAL-STRIPLINE CONFIGURATION

In the preceding section, we successfully determined the S-parameters of the dual-stripline channel on an organic substrate. The channel's characteristics, encompassing insertion loss, return loss, and crosstalk effects, comprehensively depict its behavior in the frequency domain. Nevertheless, for a more comprehensive analysis of the channel's performance in

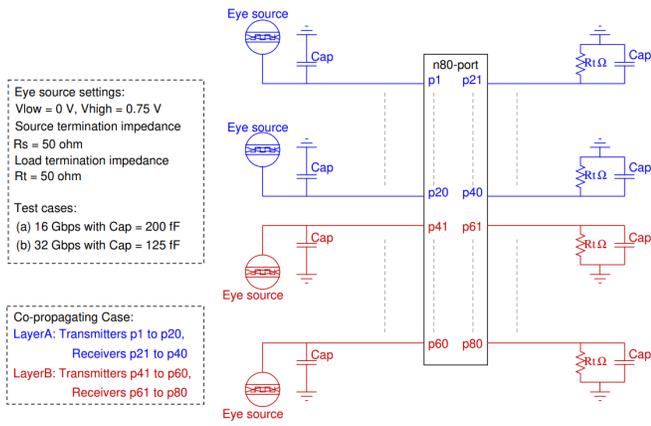


Fig. 9. Statistical eye simulation setup for the dual-stripline structure in the co-propagating case.

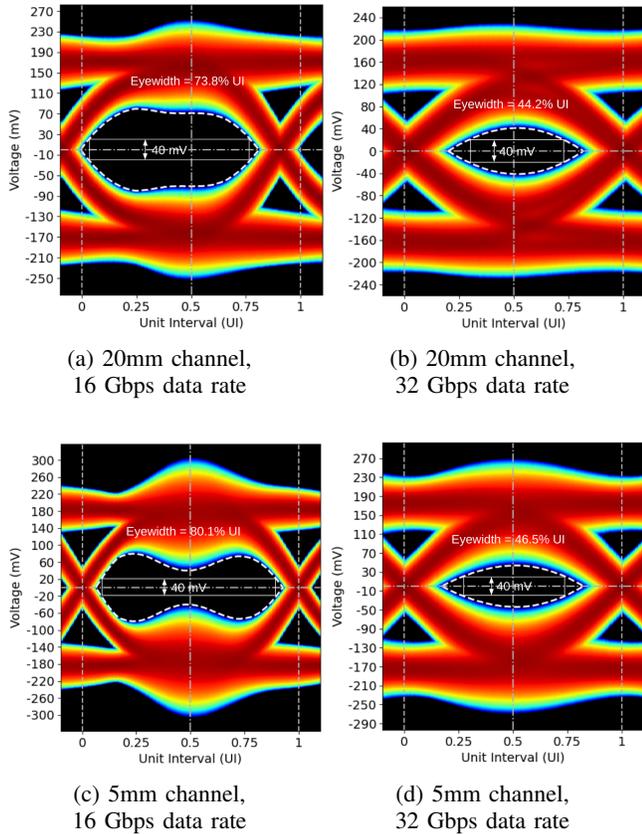


Fig. 10. Statistical eye diagrams for dual-stripline channels in co-propagating case: T-lines-only model on an organic substrate.

the time domain with higher data rate signals, we conducted statistical eye simulations employing the Seasim tool. The statistical eye simulation tool furnishes BER contours for specified bit-error rates. Fig. 9 illustrates the setup of input and output ports, as well as the input signal parameters for the statistical eye simulation. For the time domain simulations, we

TABLE III
 COMPARISON OF EYE-OPENING VALUES

Eye width in unit interval (UI) with 40 mV sensitivity				
Structure (T-lines models)	Pitch (μm)	Length (mm)	Cap = 200fF	Cap = 125fF
			16 Gbps	32 Gbps
Dual-Stripline	130	20	73.80%	44.20%
		5	80.10%	46.50%
	150	20	73.80%	44.20%
		5	82.70%	55.00%

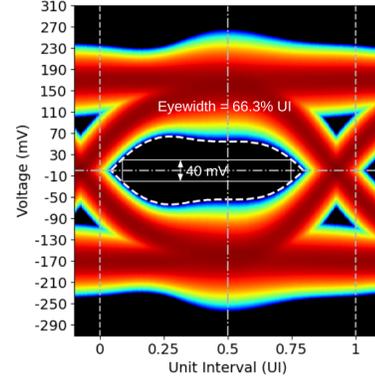


Fig. 11. Statistical eye diagram of dual-stripline channel in co-propagating case: Full model in an organic substrate, 20 mm channel with 16 Gbps data rate.

exclusively examined the co-propagating scenario, where all transmitters are on one side, rendering only the FEXT effect pertinent. Both 16 Gbps and 32 Gbps input data rates were utilized for testing the dual-stripline structure. In the case of 16 Gbps, the load side and source side were terminated with 200 fF capacitors, while for 32 Gbps, 125 fF capacitors were used. Measurement of the output is performed at the midline (Port30, i.e., CK+ in LayerA, as depicted in Fig. 3(a)). The corresponding eye diagrams for a T-lines-only model are displayed in Fig. 10. The measurements of eye-opening values were taken at a bit error rate (BER) of 10^{-15} with a voltage sensitivity of 40 mV. The obtained values are tabulated in Table III. Observing Fig. 10, it is evident that at a data rate of 16 Gbps, both the 5 mm and 20 mm channels meet the specified criterion of exceeding 50% eye-opening. As the channel length reduces from 20 mm to 5 mm, the eye widens by 6.3% unit interval (UI) for a voltage sensitivity of 40 mV. With an escalation in data rate to 32 Gbps, the eye closure intensifies, plummeting below 50% of the UI. Interestingly, increasing the bump pitch to 150 μm for a 5 mm channel at a 32 Gbps data rate results in an 8.5% expansion of the eye-opening values in a T-lines-only model. This demonstrates the effectiveness of elevating the bump pitch to 150 μm , making the dual-stripline model suitable for routing within an organic substrate. Therefore, the dual-stripline with a slightly relaxed pitch can be extended to meet UCIE standards in an organic substrate. Additionally, for a 20 mm dual-stripline channel the incorporation of bumps and vias into the T-lines-only model

diminishes the eye width by 7.5% UI, as illustrated in Fig. 11, yet remains within specified limits for a data rate of 16 Gbps.

These S-parameter values and time domain simulation results demonstrate that the dual-stripline configuration can be adopted using the co-propagating mode for organic substrates. However, due to higher NEXT levels, the dual-stripline is less suitable for use in the counter-propagating case.

V. CONCLUSION

A dual-stripline routing strategy for high-density interconnects will meet the growing demand for higher data transfer rates by increasing the number of signal layers. In general, the overall routing density can be increased up to 33% while transitioning from single-stripline to dual-stripline configuration. The dual-stripline configuration routing on the organic substrate package has been considered. An optimal routing strategy involving a half wire-to-wire pitch offset between adjacent layer traces is proposed, to overcome increased crosstalk effects due to adjacent signal layers. It is found that with this half-pitch offset routing, the inter-layer FEXT effect can be reduced. Also increasing the bump pitch from 130 μm to 150 μm makes the dual-stripline configuration work up to 32 Gbps. The dual-stripline configuration with the co-propagating case could be a viable option to increase the routing density. The S-parameters and time domain results validate that performance metrics such as crosstalk, and horizontal eye-opening requirements are met with an acceptable performance.

VI. ACKNOWLEDGEMENT

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